Cisco 2500 Series Router Architecture

Document ID: 5750

Contents

Introduction

This document provides an overview of the hardware and software architecture of the Cisco 25xx Series Routers.

Prerequisites

Requirements

There are no specific requirements for this document.

Components Used

The information in this document is based on the Cisco 25xx Series Routers.

The information in this document was created from the devices in a specific lab environment. All of the devices used in this document started with a cleared (default) configuration. If your network is live, make sure that you understand the potential impact of any command.

Conventions

For more information on document conventions, refer to the Cisco Technical Tips Conventions.

Hardware Overview

This section covers the hardware aspects of the Cisco 25xx Series Routers.

Chassis

The Cisco 25xx Series Routers can be divided into these categories.

Single LAN Chassis

Cisco 2501-2504 and 2520-2523 have a CPU motherboard with an onboard LAN (Ethernet/TokenRing) and multiple WAN ports, and a single power supply, as shown in figure 1.

Figure 1 – Chassis Rear View Sample: Cisco 2504

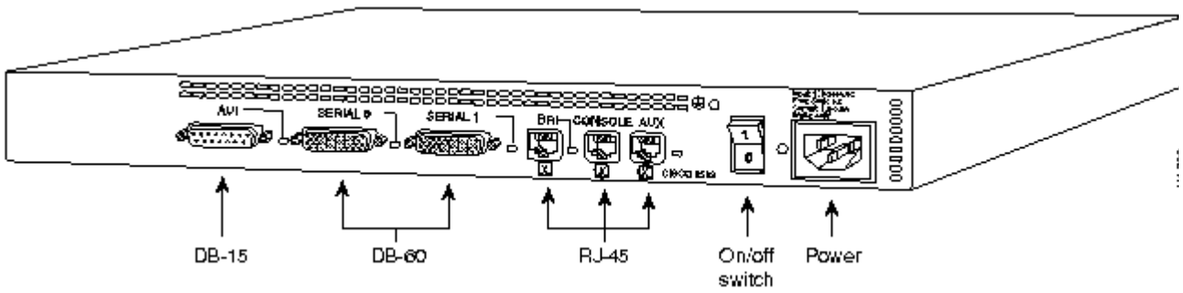


Table 1 – Summary of Single LAN Router Network Interfaces

Model	Ethernet	Token Ring	Low-Speed Serial	Serial	ISDN BRI
Cisco 2501	1	0	0	2	0
Cisco 2502	0	1	0	2	0
Cisco 2503	1	0	0	2	1
Cisco 2504	0	1	0	2	1
Cisco 2520	1	0	2	2	1
Cisco 2521	0	1	2	2	1
Cisco 2522	1	0	8	2	1
Cisco 2523	0	1	8	2	1

Hub Chassis

Cisco 2505, 2507, and 2516 have a CPU motherboard with an on-board LAN (Ethernet) with hub ports and multiple WAN ports, and a single power supply, as shown in figure 2.

Figure 2 – Chassis Rear View Sample: Cisco 2516

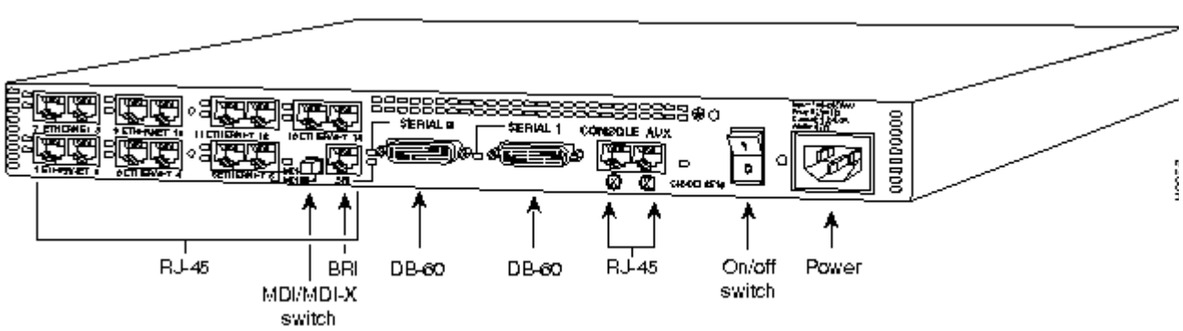


Table 2 – 10BaseT Hub Ports for Cisco 2500 Series with Hub Chassis

Model	Serial	Hub Ports	ISDN BRI
Cisco 2505	2	8	0
Cisco 2507	2	16	0
Cisco 2516	2	14	1

For more details on Cisco 2505/2507/2516 Series Routers, see Cisco 2500 Family of Hub/Routers.

Access Server Chassis

Cisco 2509-2512 have a CPU motherboard with an on-board LAN (Ethernet/Token Ring) and multiple WAN and asynchronous ports, and a single power supply, as shown in figure 3.

Figure 3 – Chassis Rear View Sample: Cisco 2511

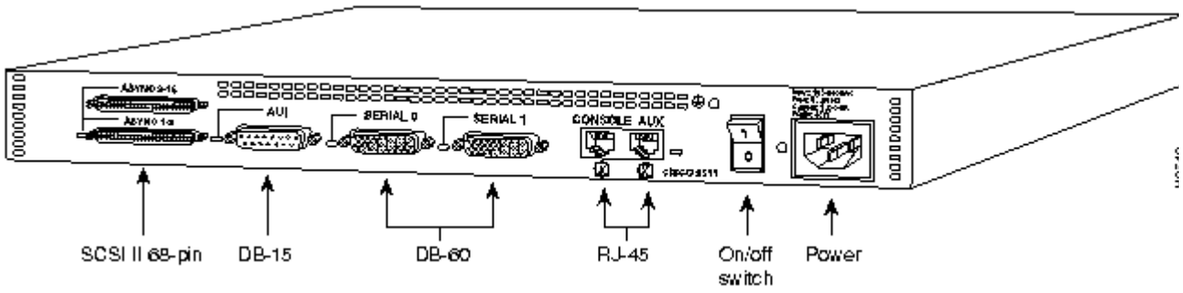


Table 3 – Ethernet, Token Ring, Serial and Async Ports for Access Servers

Model	Ethernet	Token Ring	Serial	Async
Cisco 2509	1	0	2	8
Cisco 2510	0	1	2	8
Cisco 2511	1	0	2	16
Cisco 2512	0	1	2	16

For more details on the Cisco 2509-2512 Series Routers, see Cisco 2509, 2510, 2511, and 2512.

Dual Lan Chassis

Cisco 2513-2515 have a CPU motherboard with on-board two LAN (Ethernet / Token Ring) and multiple WAN ports, and a single power supply, as shown in figure 4.

Figure 4 – Chassis Rear View Sample: Cisco 2514

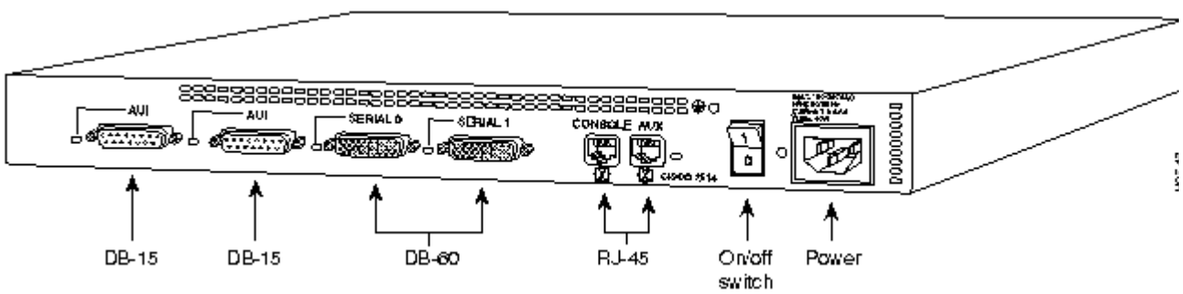


Table 4 – Dual LAN Router Interface Options

Model	Ethernet	Token Ring	Serial

Cisco 2513	1	1	2
Cisco 2514	2	0	2
Cisco 2515	0	2	2

Smart Hub Chassis

Cisco 2517-2519 have a CPU motherboard with on-board LAN (Ethernet / Token Ring) with hub ports and multiple WAN ports, a Management module, and a single power supply, as shown in figure 5.

Figure 5 – Chassis Rear View Sample: Cisco 2518

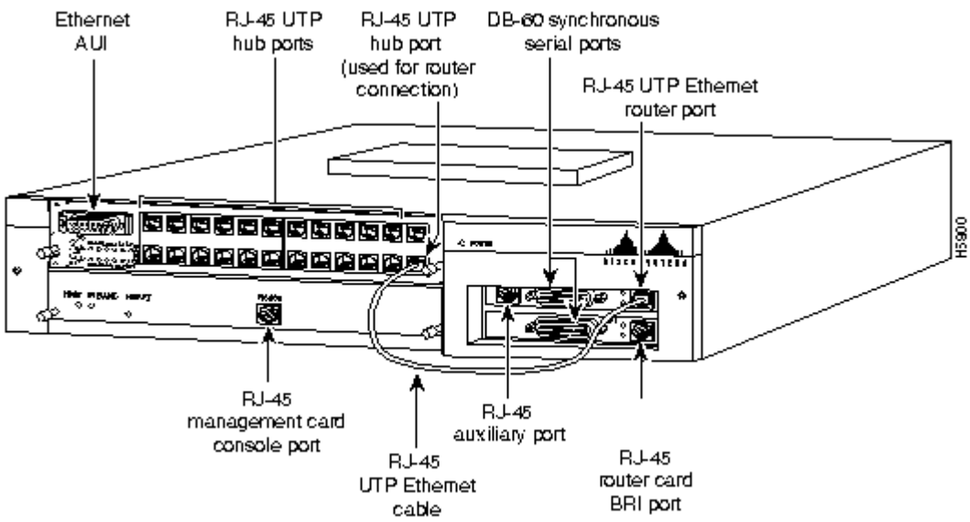


Table 5 – Smart Hub Interface Options

Model	Ethernet	Serial	Async	Hub ports (Ethernet/Token Ring)	ISDN BRI
Cisco 2517	-	2	1	12 (Token Ring)	1
Cisco 2518	1	2	1	23 (Ethernet)	1
Cisco 2519	-	2	1	24 (Token Ring)	1

For more information on the Cisco 2517/2519 Series Routers, see Cisco 2517 and Cisco 2519 Router/Hub User Guide.

For more information on the Cisco 2518 Series Router, see Cisco 2518 Router/Hub User Guide.

Modular Chassis

Cisco 2524 and 2525 have a CPU motherboard with on-board LAN (Ethernet/Token Ring) and multiple WAN ports, three slots for WAN Interface Cards (WICs), and a single external power supply, as shown in figure 6.

Figure 6 – Chassis Rear View Sample: Cisco 2524

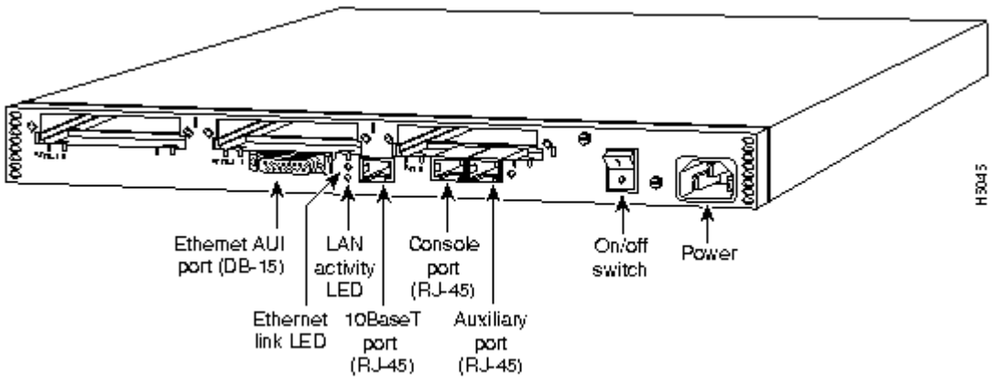


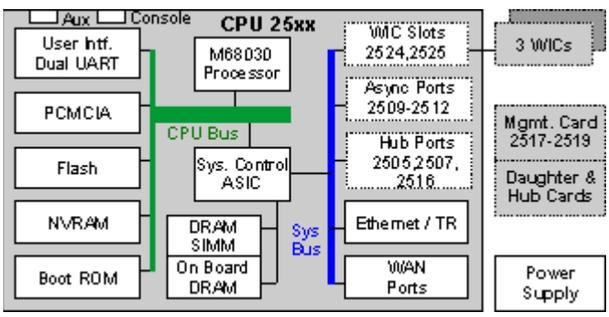
Table 6 – Modular Router Interface Options

Model	Ethernet	Token Ring	WAN Modules
Cisco 2524	1	0	3
Cisco 2525	0	1	3

For more information on the Cisco 2524/2525 Series Routers, see Cisco 2524 and Cisco 2525 Router User Guide.

CPU and Block Diagram

Figure 7 – Block Diagram



Processor

The CPU used in the 25xx Series is a Motorola 68030 CISC. The characteristics of the CPU are:

- 32 bit bus, 20 MHz clock (25 MHz on some platforms).
- 256 Bytes internal Data Cache, 256 Bytes internal Instruction Cache, both direct mapped.

System Control Logic

System Control Logic helps the main processor with device control, interrupt handling, counting and timing, data transfer, minimal First In, First Out (FIFO) buffering, and communication with network interfaces and Dynamic RAM (DRAM).

25xx Series platforms use Anchor Application Specific Integrated Circuit (ASIC) for data transfer to DRAM and System Bus, and Steam ASIC for accessing network interface devices. These are shown as System Control ASICs (one block) in the above diagrams.

Network Interfaces

Network Interfaces provide on board data transfer functionality.

- Each 25xx router has an on-board Ethernet/Token Ring controller, and Serial Communication Channels (SCC) for WAN ports.
- WIC slots provide further modularity for WAN interfaces on the 2524 and 2525.

Wan Interface Cards

Wan Interface Cards (WIC) are media specific network interfaces (only on the 2524 and 2525) responsible for data transfer in and out of the 25xx series router, (in addition to the on-board interfaces).

- The WIC communicates with the CPU through the System Bus for packet transfer.
- Specialized controllers (or ASICs) used for media support perform the above mentioned functionality.
- WICs do not support online insertion and removal (OIR).
- Cisco IOS® software is revised as new WICs are designed. Ensure that you use the release of Cisco IOS software that contains code for any hardware in the router.

Buses

Buses are used by the CPU to access various components of the system, and transfer instructions and data to or from specified memory addresses.

- **CPU Bus** is for high speed operations, with direct Processor access - 32 bit address and 32 bit data, 20 MHz. These include access to Dual Universal Asynchronous Receiver/Transmitter (UART), Boot ROM, nonvolatile RAM (NVRAM), Flash, and PCMCIA Flash.
- **System Bus** allows communication with Ethernet/Token Ring controllers, WAN port interfaces, and so on.
- DRAM is accessed through System Control ASICs and allows Direct Memory Access (DMA).

Dual UART

Dual Universal Asynchronous Receiver-Transmitter (UART) provides the necessary user interface. It has one RS232 port, Data Communications Equipment (DCE) (Console) RJ45, and Data Terminal Equipment (DTE) (Aux) RJ45.

Power supply provides power to various components of the router.

Memory Details

This section describes memory details of the Cisco 25xx Series routers.

DRAM

The DRAM is divided in Main Processor Memory and Shared Input/Output (I/O) memory.

- Main Processor Memory is used for routing tables, fast switching cache, running configuration, and so on. It can take unused shared I/O memory, if needed.
- Shared I/O memory is used for temporary storage of packets in system buffers.
- Physically, all the boards have one single inline memory module (SIMM) slot (72-pin, 70 ns). Furthermore, if the revision level of the board is A through G, there are an additional 2 MB of RAM soldered to the system card. If the revision level is I through N, there is no RAM soldered to the system card.

  Use the **show version** command to check the board revision number and the different types of memory:

```
Cisco Internetwork Operating System Software
IOS (tm) 2500 Software (C2500-JS-L),
Version 12.2(27), RELEASE SOFTWARE (fc3)
Copyright (c) 1986-2004 by cisco Systems, Inc.
Compiled Tue 02-Nov-04 22:01 by kellmill
```

```
Image text-base: 0x0307D390, data-base: 0x00001000
ROM: System Bootstrap, Version 11.0(10c), SOFTWARE
BOOTLDR: 3000 Bootstrap Software (IGS-BOOT-R),
Version 11.0(10c), RELEASE SOFTWARE (fc1)

R1 uptime is 2 weeks, 4 days, 9 hours, 12 minutes
System returned to ROM by reload
System image file is "flash:/c2500-js-l.122-27.bin"

cisco 2500 (68030) processor (revision N) with 14336K/2048K
bytes of memory.
Processor board ID 19484205, with hardware revision 00000000
Bridging software.
X.25 software, Version 3.0.0.
SuperLAT software (copyright 1990 by Meridian Technology Corp).
TN3270 Emulation software.
1 Ethernet/IEEE 802.3 interface(s)
2 Serial network interface(s)
32K bytes of non-volatile configuration memory.
16384K bytes of processor board System flash (Read ONLY)
```

Configuration register is 0x2102.

- DRAM SIMM can be up to 16 MB, so total DRAM can be 18 MB on routers having an additional 2 MB on-board.
- If the SIMM is not used, shared I/O memory is 1 MB and Main Processor Memory is 1 MB of the 2 MB on-board DRAM.
- If SIMM is used, shared I/O memory is 2 MB on-board DRAM, and Main Processor Memory is the SIMM (up to 16 MB).
- For the 25xx platforms that do not have on-board DRAM and only use SIMMs, the memory is logically divided in shared I/OmMemory and main processor memory.

Flash

Flash provides permanent storage of the Cisco IOS software image, backup configurations, and any other files.

- Flash on 25xx is implemented using two SIMMs (80-pin, 120 ns).
- Flash size can be 4, 8, or 16 MB.
- The 2500 routers run the Cisco IOS software from Flash. These image files are defined as re-locatable, because the Cisco IOS software image can be executed from different locations in the Flash.

  A re-locatable image file is recognized by the letter "l" contained in the file name (for instance: c2500-js-l.121-9). As a consequence, the Flash memory is set as **read only** when the main Cisco IOS software is running. Copying a new Cisco IOS software image then requires the router to be in RxBoot. Newer releases of Cisco IOS software make this step automatic and transparent in the background.

NVRAM

NVRAM is used for writeable permanent storage of the startup configuration. NVRAM size is 32 KB.

BOOT ROM

This refers to erasable programmable read-only memory (EPROM) used to permanently store the startup diagnostic code (ROM Monitor), and RxBoot. Boot ROM size is 2 MB.

ID PROM

ID PROM, also known as EPROM (size 256 bytes) is used for permanent storage of the hardware

revision and identification information, as well as the MAC addresses for LAN interfaces.

Boot Sequence

Here is a typical boot sequence on a 2514 router:

The system bootstrap software (boot image) executes and searches for a valid Cisco IOS software image. The source of the Cisco IOS software image (Flash memory or a Trivial File Transfer Protocol (TFTP) server) is determined by the configuration register setting. The factory-default setting for the configuration register is 0x2102, which indicates that the router should attempt to load a Cisco IOS software image from Flash memory.

```
System Bootstrap, Version 11.0(10c), SOFTWARE
Copyright (c) 1986-1996 by cisco Systems
2500 processor with 16384 Kbytes of main memory
F3: 14732748+962056+889336 at 0x3000060
```

When a valid Cisco IOS software image is found, the router boots the software (remember that on the 25xx, the Cisco IOS software image runs from Flash memory):

```
           Restricted Rights Legend
Use, duplication, or disclosure by the Government is
subject to restrictions as set forth in subparagraph
(c) of the Commercial Computer Software - Restricted
Rights clause at FAR sec. 52.227-19 and subparagraph
(c) (1) (ii) of the Rights in Technical Data and Computer
Software clause at DFARS sec. 252.227-7013.
           cisco Systems, Inc.
           170 West Tasman Drive
           San Jose, California 95134-1706
Cisco Internetwork Operating System Software
IOS (tm) 2500 Software (C2500-JS-L), Version 12.2(10b),
RELEASE SOFTWARE (fc1)
Copyright (c) 1986-2002 by cisco Systems, Inc.
Compiled Fri 12-Jul-02 02:13 by pwade
Image text-base: 0x0307AA24, data-base: 0x00001000
cisco 2500 (68030) processor (revision F) with 16384K/2048K
bytes of memory.
Processor board ID 04796554, with hardware revision 00000000
Bridging software.
X.25 software, Version 3.0.0.
SuperLAT software (copyright 1990 by Meridian Technology Corp).
TN3270 Emulation software.
Basic Rate ISDN software, Version 1.1.
1 Ethernet/IEEE 802.3 interface(s)
2 Serial network interface(s)
1 ISDN Basic Rate interface(s)
32K bytes of non-volatile configuration memory.
16384K bytes of processor board System flash (Read ONLY)
Press RETURN to get started!
```

The last stage is the initialization of the interfaces and the message %SYS-5-RESTART: System restarted.

```
00:00:10: %LINK-3-UPDOWN: Interface Ethernet0, changed state to up
00:00:10: %LINK-3-UPDOWN: Interface Serial0, changed state to up
00:00:10: %LINK-3-UPDOWN: Interface Serial1, changed state to down
00:00:11: %LINEPROTO-5-UPDOWN: Line protocol on Interface Serial0,
 changed state to up
00:00:19: %LINEPROTO-5-UPDOWN: Line protocol on Interface Ethernet0,
 changed state to up
00:00:28: %LINEPROTO-5-UPDOWN: Line protocol on Interface Ethernet0,
 changed state to up
00:00:30: %LINK-5-CHANGED: Interface Serial0,
 changed state to administratively down
00:00:31: %LINEPROTO-5-UPDOWN: Line protocol on Interface Serial0,
 changed state to down
00:00:31: %LINK-5-CHANGED: Interface BRI0,
 changed state to administratively down
00:00:32: %LINEPROTO-5-UPDOWN: Line protocol on Interface BRI0,
 changed state to down
00:00:32: %SYS-5-CONFIG_I: Configured from memory by console
00:00:33: %LINK-5-CHANGED: Interface Serial1,
```

```
 changed state to administratively down
00:00:36: %LINEPROTO-5-UPDOWN: Line Route protocol on Interface Serial1,
 changed state to
   down
00:01:16: %SYS-5-RESTART: System restarted --
Cisco Internetwork Operating System Software
IOS (tm) 2500 Software (C2500-JS-L), Version 12.2(10b),
RELEASE SOFTWARE (fc1)
Copyright (c) 1986-2002 by cisco Systems, Inc.
Compiled Fri 12-Jul-02 02:13 by pwade
00:01:16: %SNMP-5-COLDSTART: SNMP agent on host Router
is undergoing a cold start>
Router>
```

Packet Switching

The switching architecture of the Cisco 25xx series, and the 1600, 4000 and AS5300, is based on shared memory architecture.

Cisco IOS software on shared memory routers uses the systems buffers for *all packet switching*, not just process switching. In addition to the standard public buffer pools, Cisco IOS software also creates private system buffer pools and special buffer structures for the interface controllers called RX rings and TX rings.

Private Buffer Pools

Private buffer pools are static and are allocated with a fixed number of buffers at Cisco IOS software initialization. New buffers cannot be created on demand for these pools. If a buffer is needed and none is available in the private pool, Cisco IOS software falls back to the public buffer pool for the size that matches the maximum transmission unit (MTU) of the interface.

Receive Rings and Transmit Rings

Cisco IOS software creates these rings on behalf of the media controllers and then manages them jointly with the controllers. Each interface has a pair of rings: a receive ring to receive packets, and a transmit ring to transmit packets.

Receive rings have a constant number of packet buffers allocated to them that equals the size of the ring. The **show controllers ethernet** command displays the size and the location of the receive and transmit rings:

```
TIC#show controllers ethernet 0
LANCE unit 0, idb 0x146AC0, ds 0x148618, regaddr = 0x2130000, reset_mask 0x2
IB at 0x606E64: mode=0x0000, mcfilter 0000/0000/0100/0000
station address 00e0.1e42.c7b0  default station address 00e0.1e42.c7b0
buffer size 1524
RX ring with 16 entries at 0x606EA8
Rxhead = 0x606ED8 (6), Rxp = 0x14864C (6)
00 pak=0x14A4E8 ds=0x60C13A status=0x80 max_size=1524 pak_size=64
01 pak=0x14ABE4 ds=0x60D56E status=0x80 max_size=1524 pak_size=64
...
TX ring with 4 entries at 0x606F68, tx_count = 0
tx_head = 0x606F80 (3), head_txp = 0x148694 (3)
tx_tail = 0x606F80 (3), tail_txp = 0x148694 (3)
00 pak=0x000000 ds=0x663746 status=0x03 status2=0x0000 pak_size=60
...
```

- **RX ring with 16 entries at 0x606EA8**—The size of the receive ring is 16, and it begins at the address 0x606EA8 in I/O memory.
- **TX ring with 4 entries at 0x606F68, tx_count = 0**—The size of the transmit ring is 16, it begins at the address 0x606F68 in I/O memory, and there are no packets to be transmitted on this interface.

Switching Paths

This description is based on the book *Inside Cisco IOS Software Architecture*, Cisco Press[1].

[1]"CCIE Professional Development: Inside Cisco IOS Software Architecture" by Vijay Bollapragada, Curtis Murphy, Russ White (ISBN 1-57870-181-3).

1 - Receive the packet

Step 1: The interface media controller detects a packet on the network media and copies it into a buffer to which the first free element in the receive ring points. Media controllers use the Direct Memory Access (DMA) method to copy packet data into memory.

Step 2: The media controller changes ownership of the packet buffer back to the processor, and issues a receive interrupt to the processor. The media controller does not have to wait for a response from the CPU, and continues to receive incoming packets into the receive ring.

It is possible for the media controller to fill the receive ring before the processor processes all the new buffers in the ring. This condition is called an overrun. When this occurs, all incoming packets are dropped until the processor recovers.

Step 3: The CPU responds to the receive interrupt, and attempts to remove the newly-filled buffer from the receive ring, and replenishes the ring from the private pool of the interface. Notice that packets are not physically moved within the I/O memory. Instead, only the pointers are changed. If the input hold queue of the interface is full, the packet is dropped; otherwise, three outcomes are possible:

- **3.1**: A free buffer is available in the private pool of the interface to replenish the receive ring. The free buffer is linked to the receive ring and the packet now belongs to the private buffers pool of the interface.
- **3.2**: A free buffer is not available in the private pool of the interface, so the receive ring falls back to the global pool that matches the MTU of the interface, in order to be replenished. The fallback counter value increases for the private pool.
- **3.3**: If a free buffer is not available in the public pool as well, the incoming packet is dropped, and the ignore counter value increases. In addition, the interface is throttled and all incoming traffic is ignored on this interface for a short period.

2 - Switch the Packet

Step 4: After the receive ring is replenished, the CPU begins to switch the packet. Cisco IOS software attempts to switch the packet with the help of the fastest method configured on the interface. On shared memory routers, it first tries Cisco Express Forwarding (CEF) switching (if configured), then fast switching (unless the **no ip route-cache** command is configured on the interface), and finally, process switching if none of the others work.

Step 5: While still in the receive interrupt context, the Cisco IOS software attempts to use the CEF table or the fast switching cache to make a switching decision. Switching can be:

- **5.1**: CEF switching—If there are valid CEF and adjacency table entries, the Cisco IOS software rewrites the Media Access Control (MAC) header on the packet and begins to transmit it (see Step 8). If there is no CEF entry for the destination, the packet is dropped.
- **5.2**: Fast switching—If CEF is not enabled or the packet cannot be CEF switched, the Cisco IOS software attempts to fast-switch the packet. If there is a valid fast cache entry for this destination, the Cisco IOS software rewrites the MAC header information and begins to transmit the packet (see Step 8). If there is no valid fast cache entry, the packet is queued for process switching (see Step 6).

Step 6: Process switching—If both CEF and fast switching fail, the Cisco IOS software falls back to process switching. The packet goes in the queue of the appropriate process (for instance, an IP packet is placed in the queue for the IP Input process), and the receive interrupt is dismissed.

Step 7: Eventually the packet switching process runs, and switches the packet and rewrites the MAC header as needed. Notice that the packet still has not moved from the buffer into which it was originally copied. After the packet is switched, the Cisco IOS software continues to the packet transmit stage.

3 - Transmit the Packet

Step 8: If the packet was CEF or fast switched, the Cisco IOS software checks to see if there are packets on the output queue of the outbound interface, while still in receive interrupt context.

- **8.1**: If there are packets already on the output hold queue for the interface, the Cisco IOS software places the packet on the output hold queue instead of directly into the transmit ring to reduce the possibility of out-of-order packets, and then proceeds to Step 8.3.
- **8.2**: If the output hold queue is empty, the Cisco IOS software places the packet on the transmit ring of the output interface. To do so, it links the packet buffer to a transmit ring descriptor. The receive interrupt is dismissed, and processing continues with Step 11. If there is no room on the transmit ring, the packet is placed on the output hold queue instead, and the receive interrupt is dismissed.
- **8.3**: If the output hold queue is full, the packet is dropped, the output drop counter value increases, and the receive interrupt is dismissed.

Step 9: If the packet was process-switched, the packet is placed on the output queue for the input interface. If the output queue is full, the packet is dropped and the output drop counter value increases.

Step 10: The Cisco IOS software attempts to find a free descriptor in the output interface transmit ring. If a free descriptor exists, the Cisco IOS software removes the packet from the output hold queue and links the buffer to the transmit ring. If the ring is full, the Cisco IOS software leaves the packet in the output hold queue until the media controller transmits a packet from the ring and frees a descriptor.

Step 11: The outbound interface media controller polls its transmit ring periodically for packets that need to be transmitted. As soon as the media controller detects a packet, it copies the packet onto the network media and raises a transmit interrupt to the processor.

Step 12: The Cisco IOS software acknowledges the transmit interrupt, de-links the packet buffer from the transmit ring, and returns the buffer to the pool of buffers from which it originated. The Cisco IOS software then checks the output hold queue for the interface. If any packets await in the output hold queue, the Cisco IOS software removes the next one from the queue and links it to the transmit ring. Finally, the transmit interrupt is dismissed.

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Network Infrastructure: WAN Routing and Switching
ISDN Problem - Feb 28, 2005 HSRP - Which multicast address? - Feb 28, 2005 MLDN CIRCUIT - Feb 28, 2005 Cat.3750 Switch Web Config Problem - Feb 28, 2005 Cisco1841 with 1MFT-E1-G.703 has AIS on Controller E1 after reload - Feb 28, 2005

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- **Software Installation and Upgrade Procedure for the 1600, 2000, 2500, 3000, AS5100, and AS5200**
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